Complementary Lithography at Insertion and Beyond

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Portland Technology Development
Intel Corporation

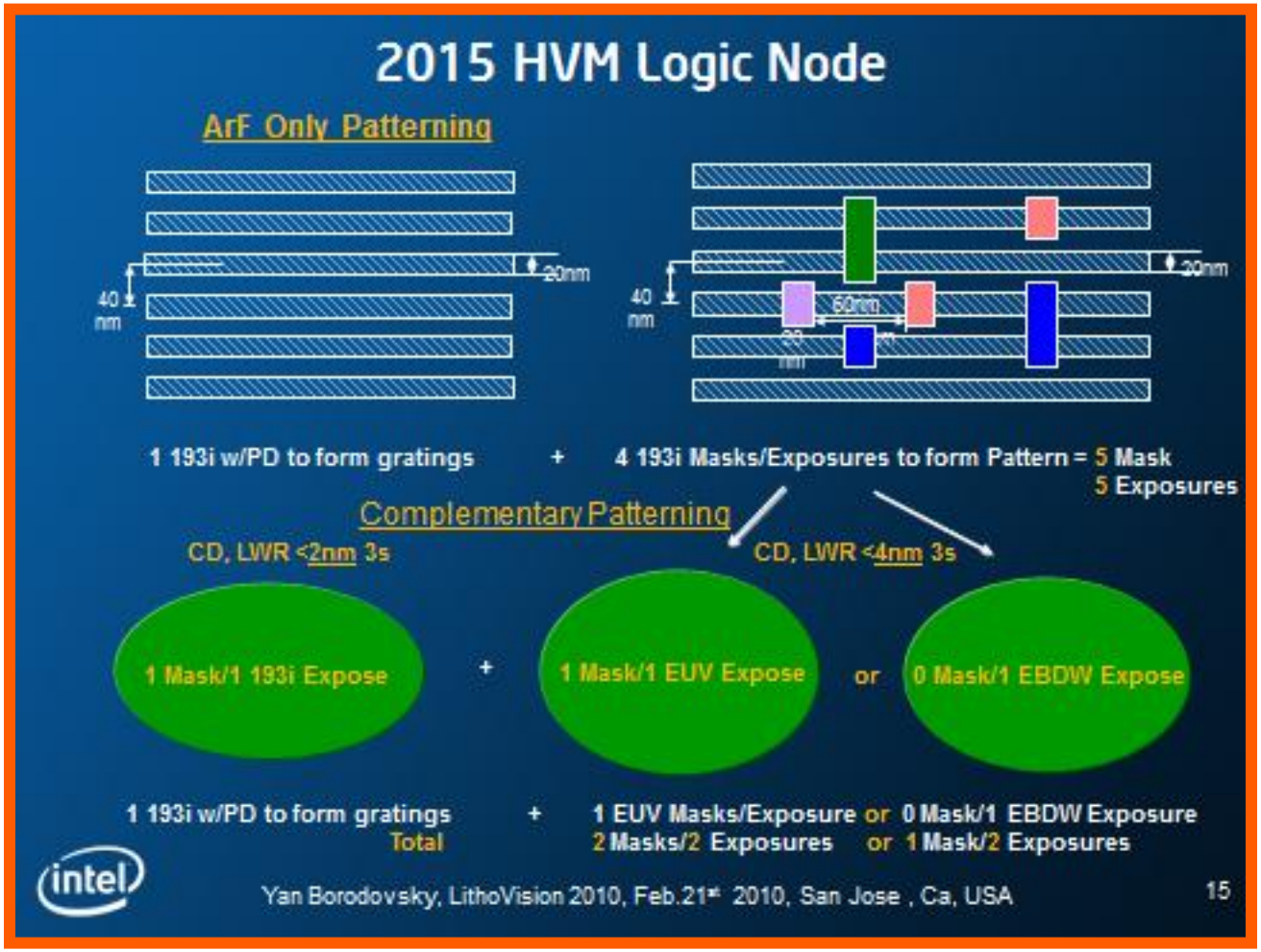
Semicon West 2012, June 11, 2012, San Francisco, CA, USA

Complementary Lithography - View 2010

Gridded Layouts –
193i + Pitch Division
n*193i + Shrink Cuts
n*193i + Shrink Vias
before HVM NGL

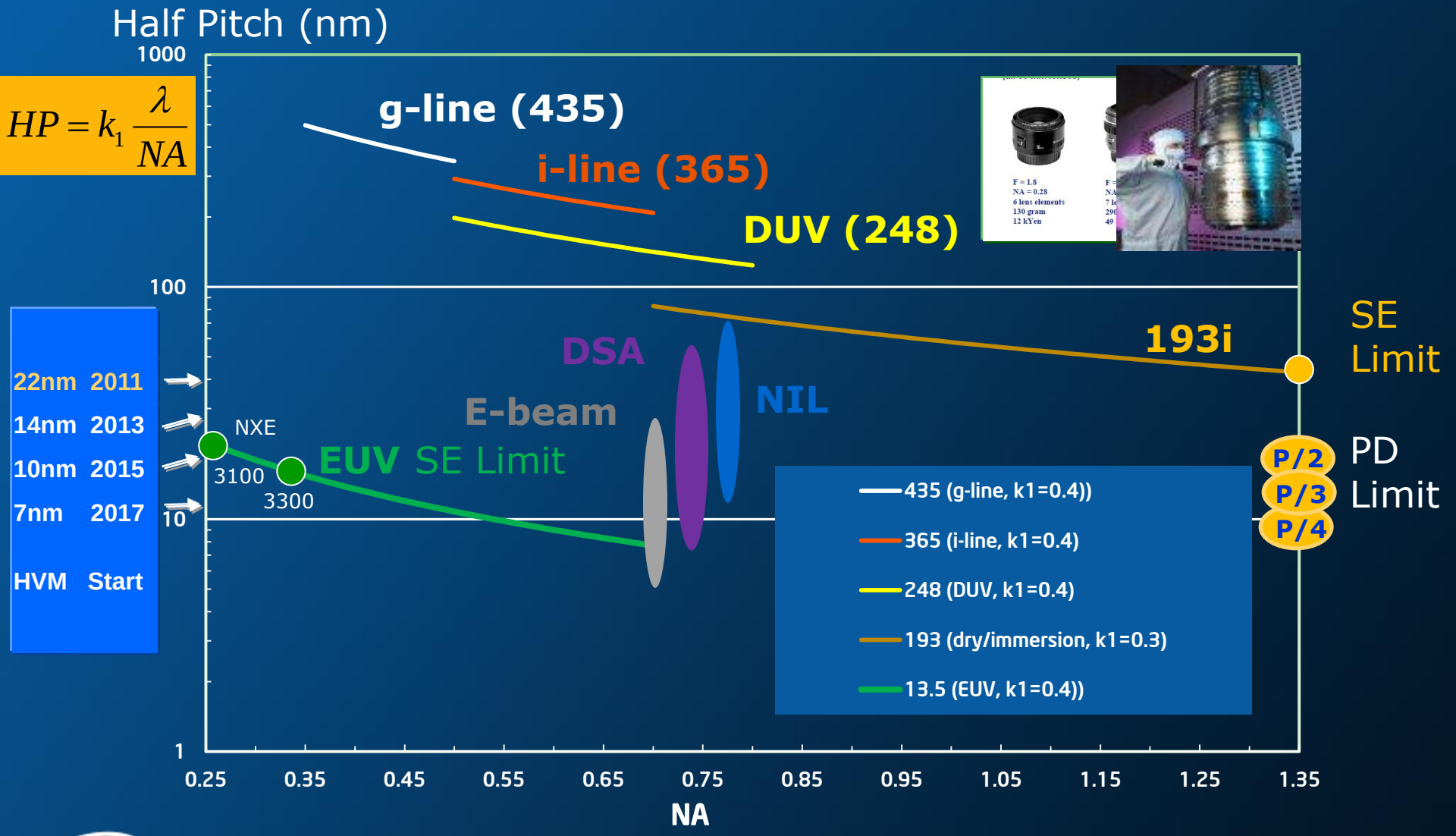
Gridded Layouts –
193i + Pitch Division
n*193i or EUV Cuts
n*193i or EUV Vias
with HVM EUV

Gridded Layouts –
193i + Pitch Division
n*193i or EBDW Cuts
n*193i or EBDW Vias
with HVM EBDW

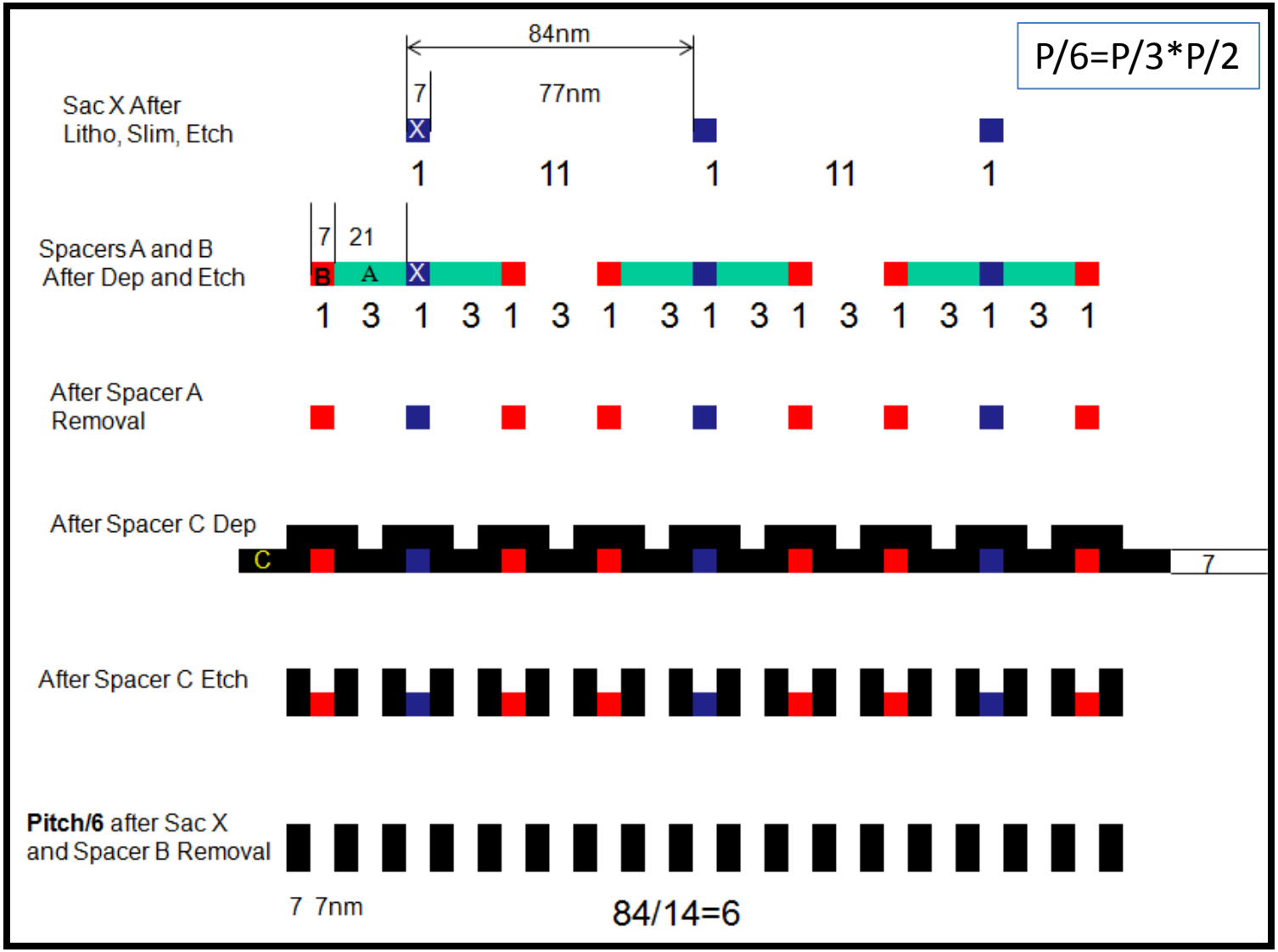


Gratings – SE and Pitch Division

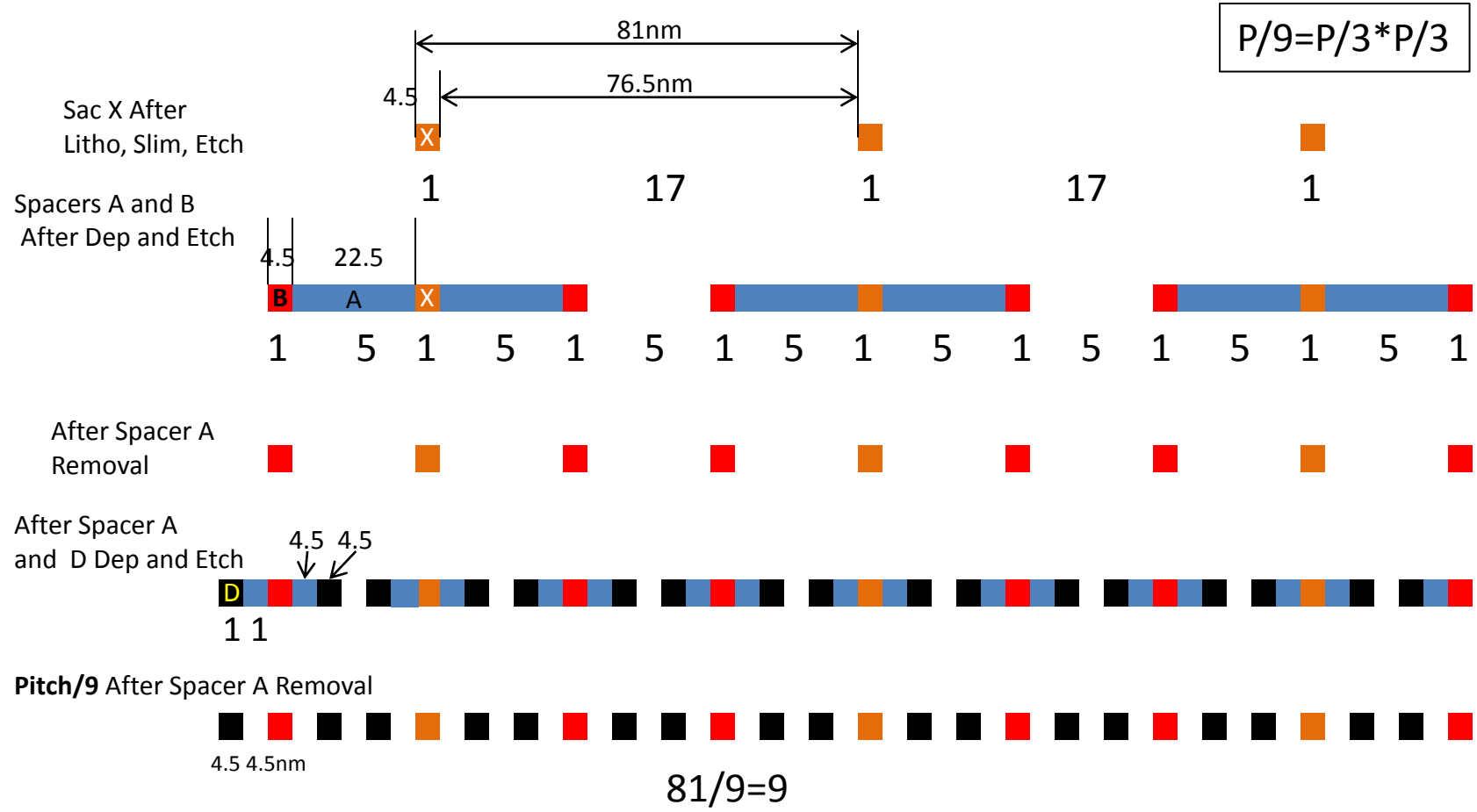
$$HP = k_1 \frac{\lambda}{NA}$$



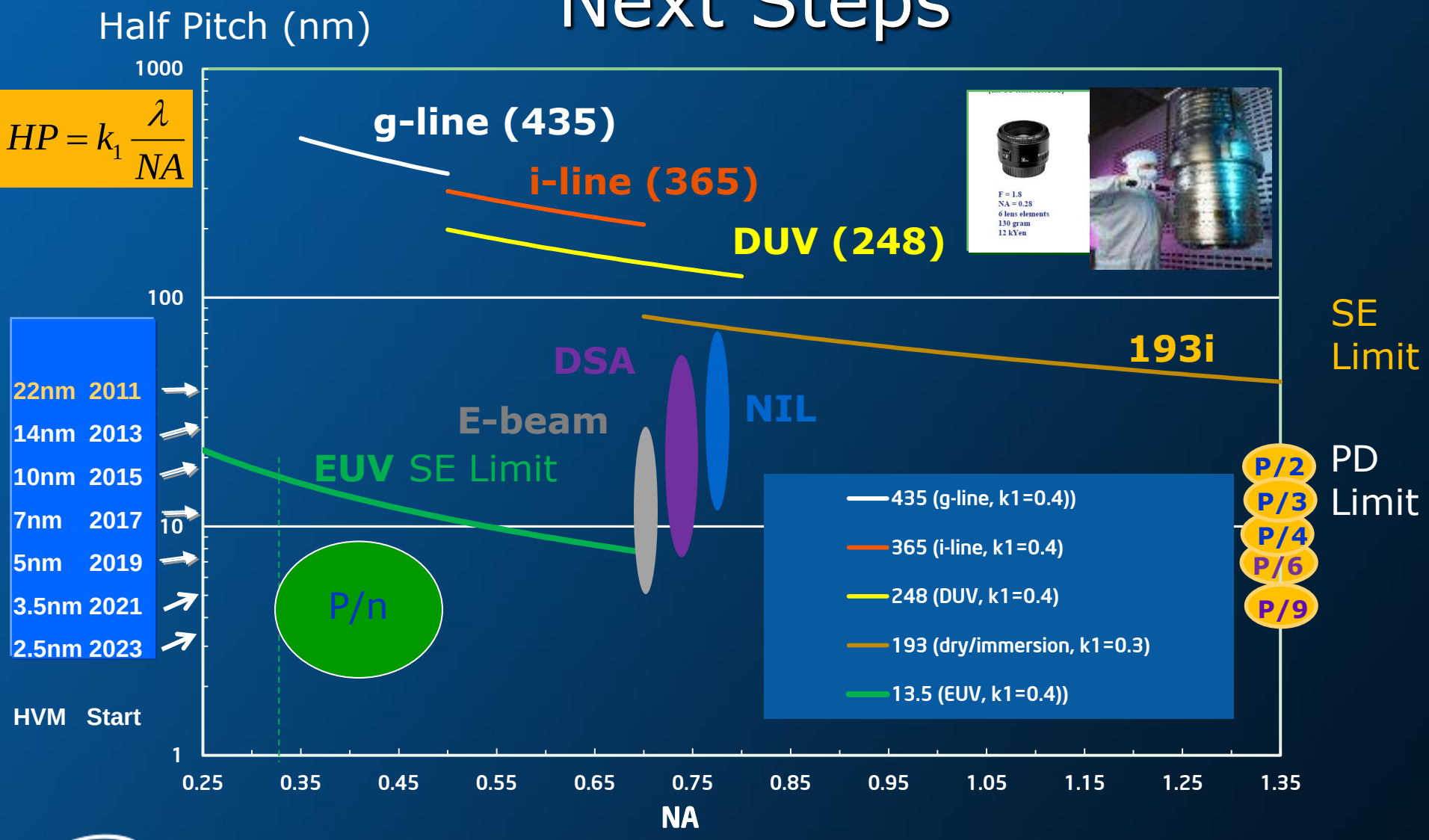
Gratings Next Steps - Pitch/6



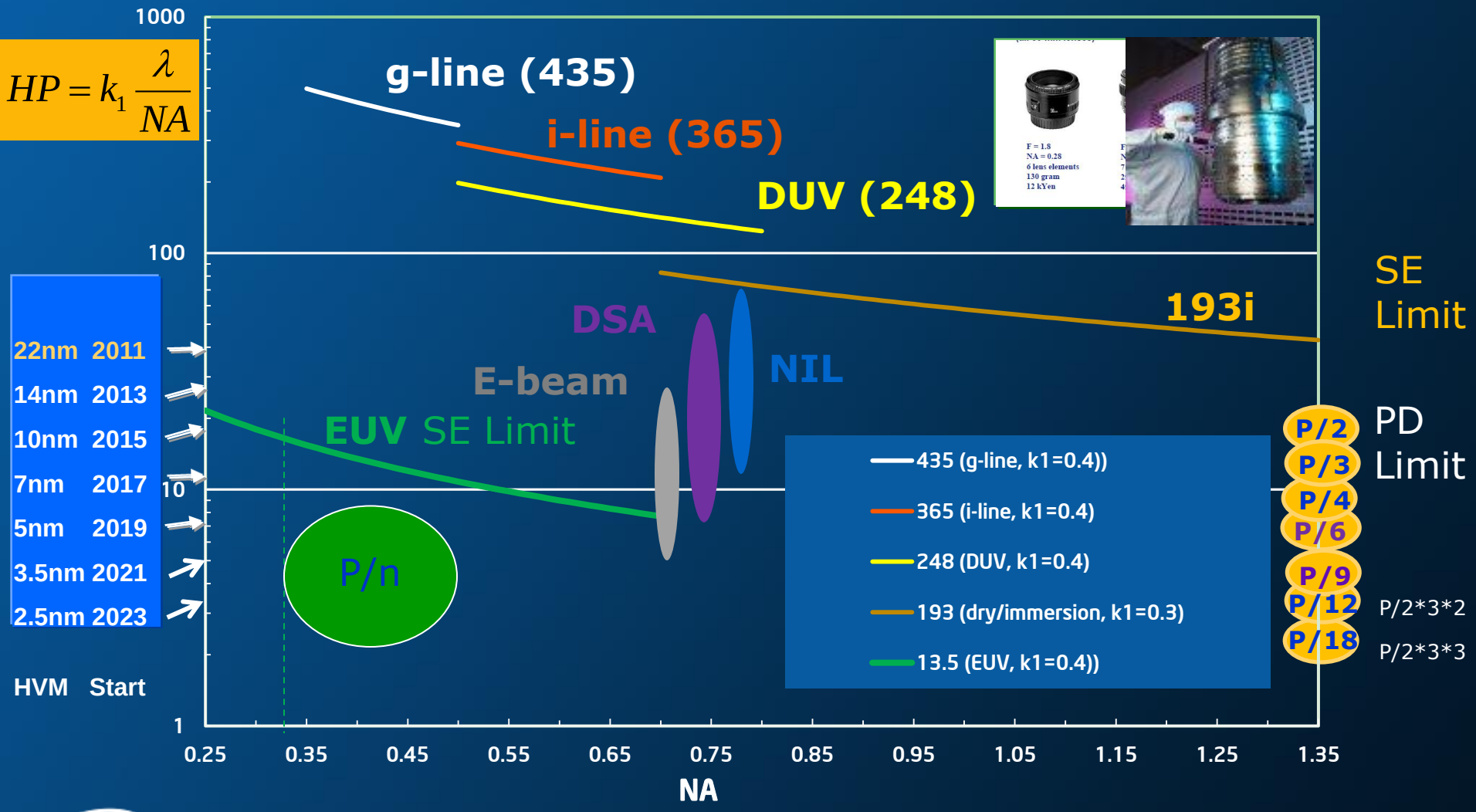
Gratings Next Steps – Pitch/9



Gratings – SE and Pitch Division Next Steps



Gratings – SE and Pitch Division Next Next Steps



Cuts and Vias - Edge Placement Errors and Stochastic Control

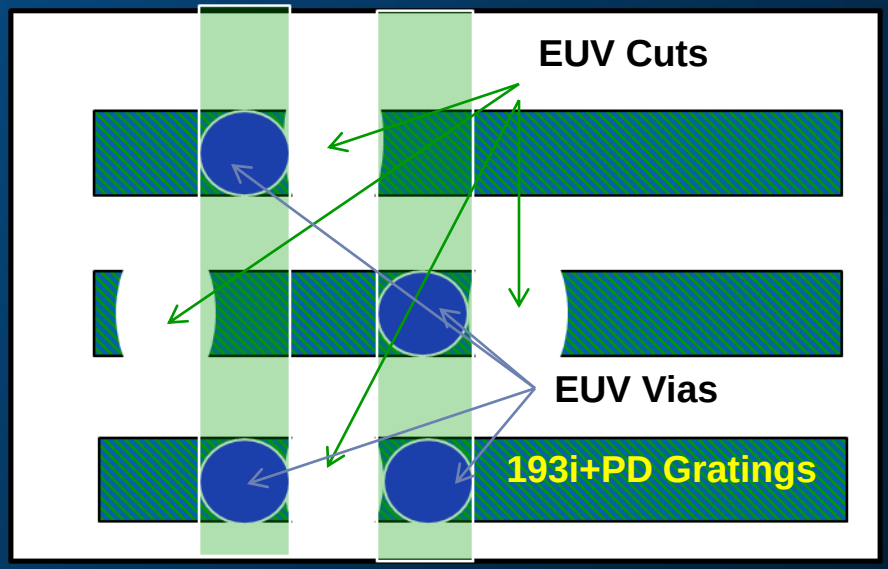
Following capabilities have to be present at HVM NGL Insertion to support Yield and COO:

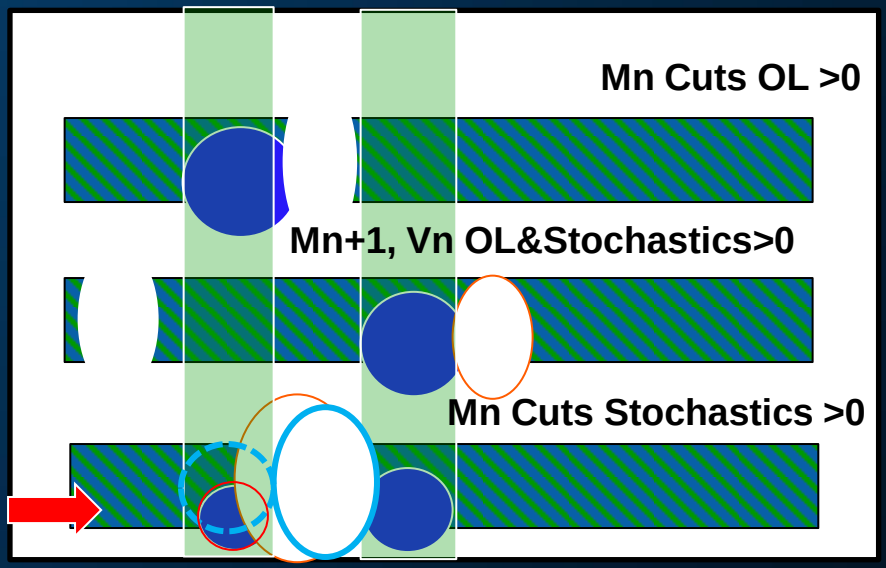
- Required Defect density/TPT
- Required NGL/193i Overlay
- Sophisticated OPC
- Stochastics Suppression

If not controlled things can get out of hand in a hurry

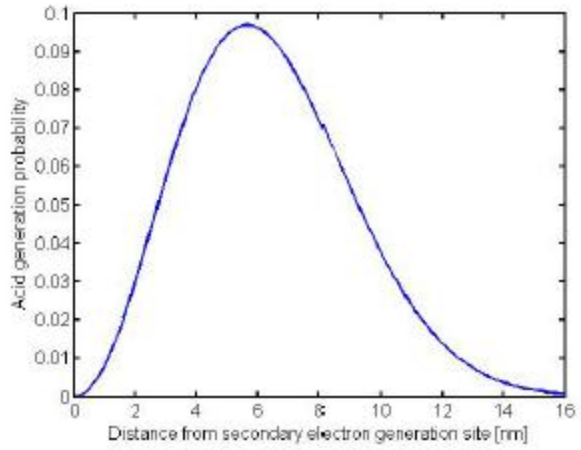
Overlay, OPC, Defects issues are known and pushed

Scope of Stochastic Suppression challenge while recognized is not addressed sufficiently.



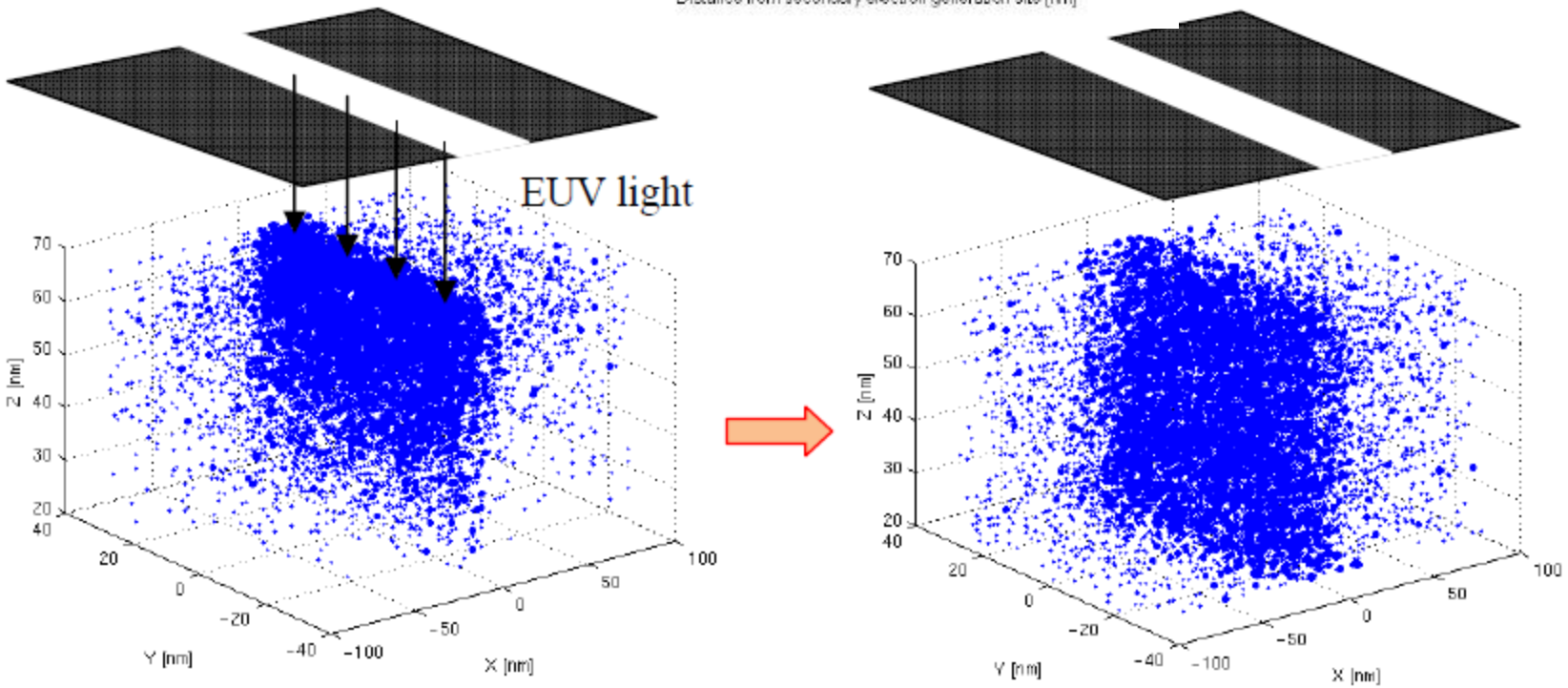


EUV Stochastics



193nm	13.4nm
15mj/cm^2	
Photons/nm^2	
145	10

Mask: a space pattern



Calibration and verification of a stochastic model for EUV resist

Weimin Gao[a,c], Alexander Philippou[b], Ulrich Klostermann[b], Joachim Siebert[b]
Vicky Philipsen[c], Eric Hendrickx[c], Tom Vandeweyer[c], Gian Lorusso[c]

Proc. of SPIE Vol. 8322 83221D-2

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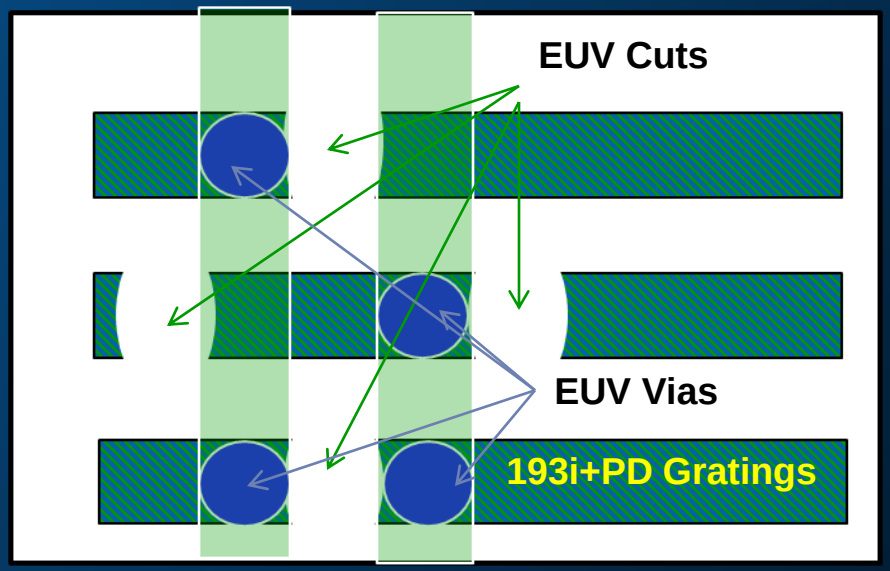
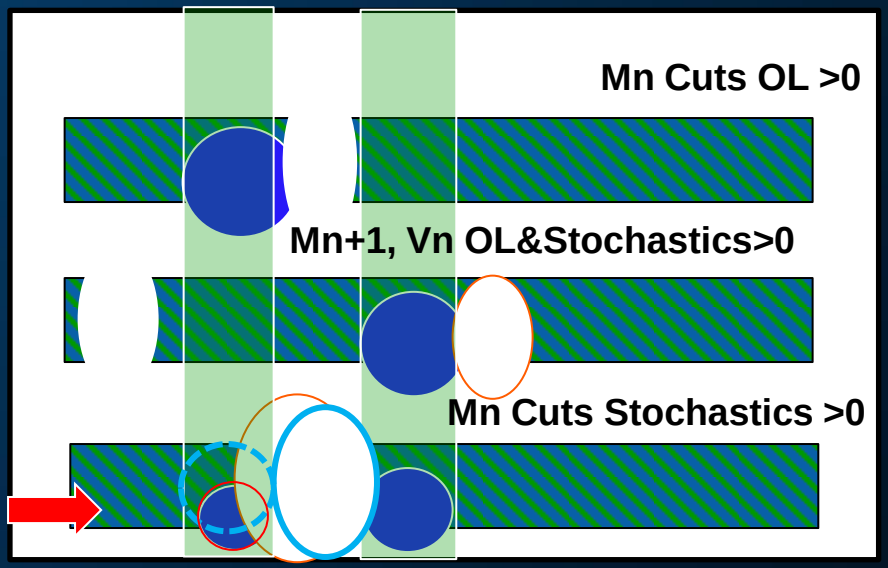
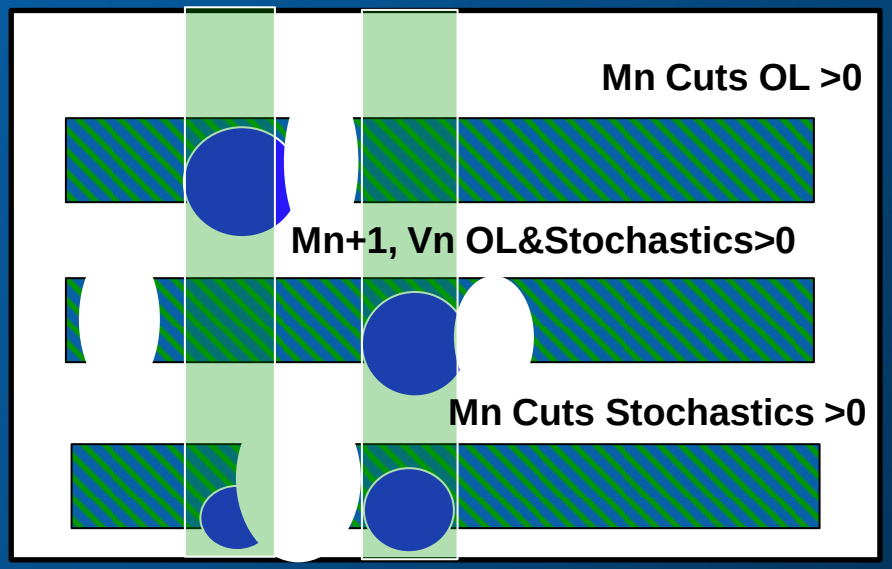


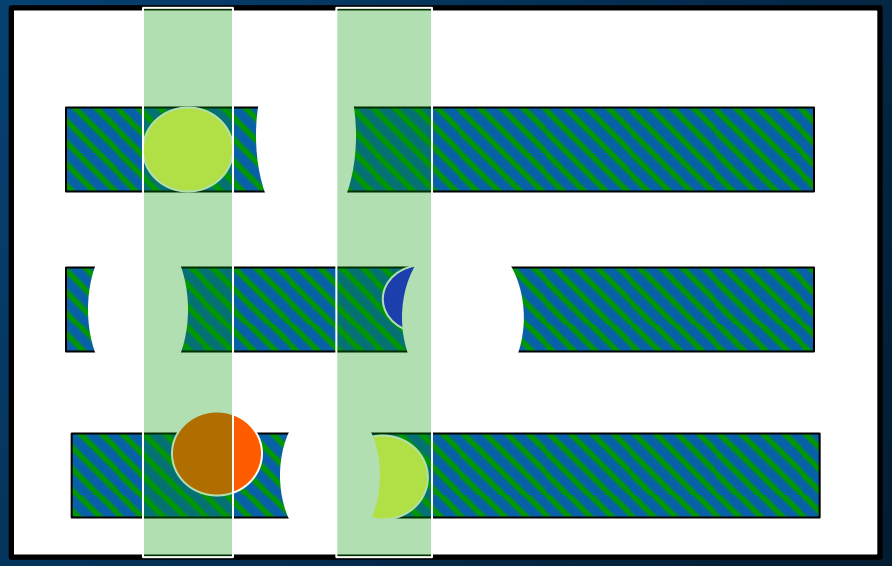


Complementary Lithography at Insertion Stochastics Suppression

EUV or EB Cuts and Vias



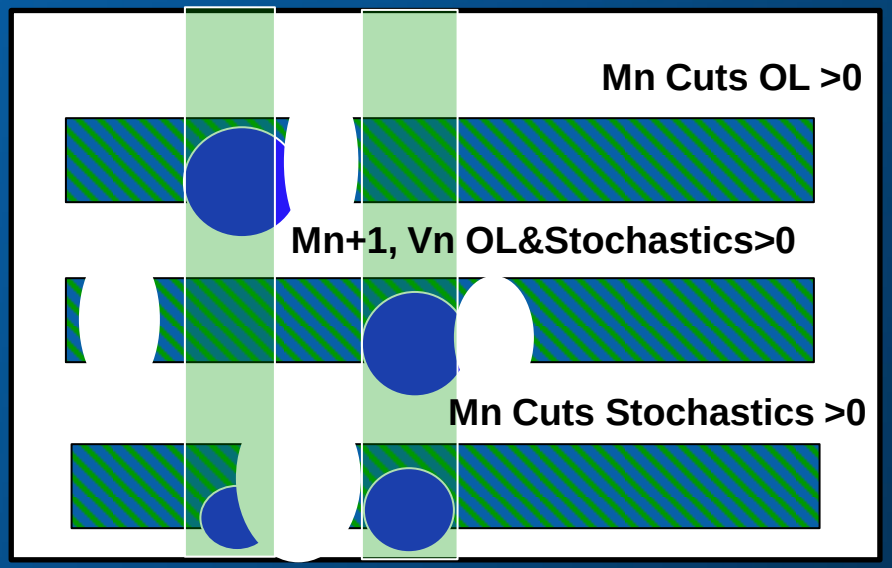
193i Cuts and Vias



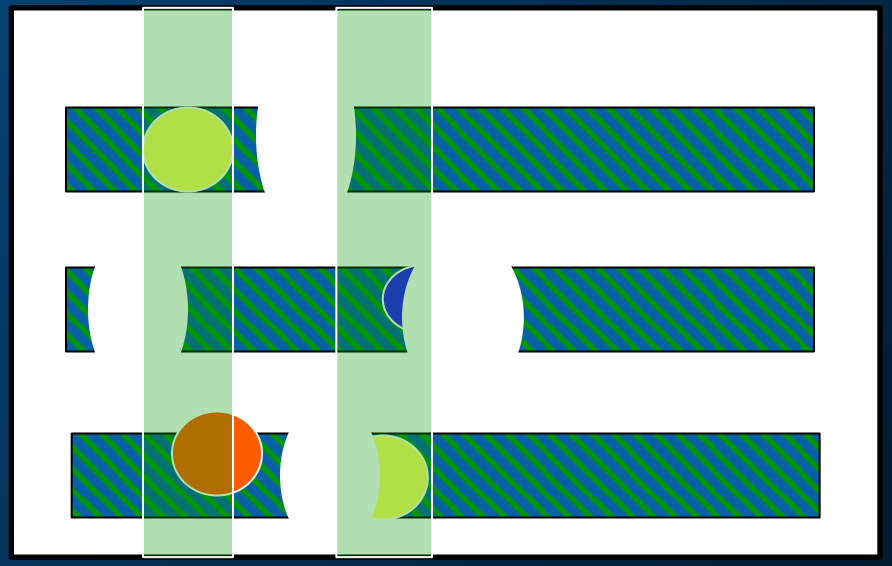
EPE (EUV or EB/193i OL) ≤ EPE (n*193i/193i OL)
EPE EUV or EB Stochastics ≥ EPE 193i Stochastic

Complementary Lithography at Insertion Stochastics Suppression

EUV or EB Cuts and Vias



193i Cuts and Vias



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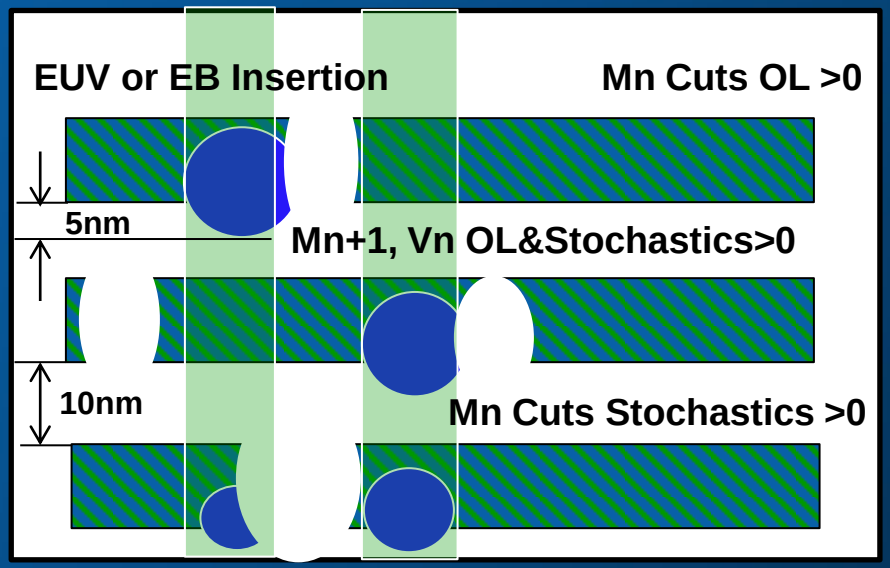
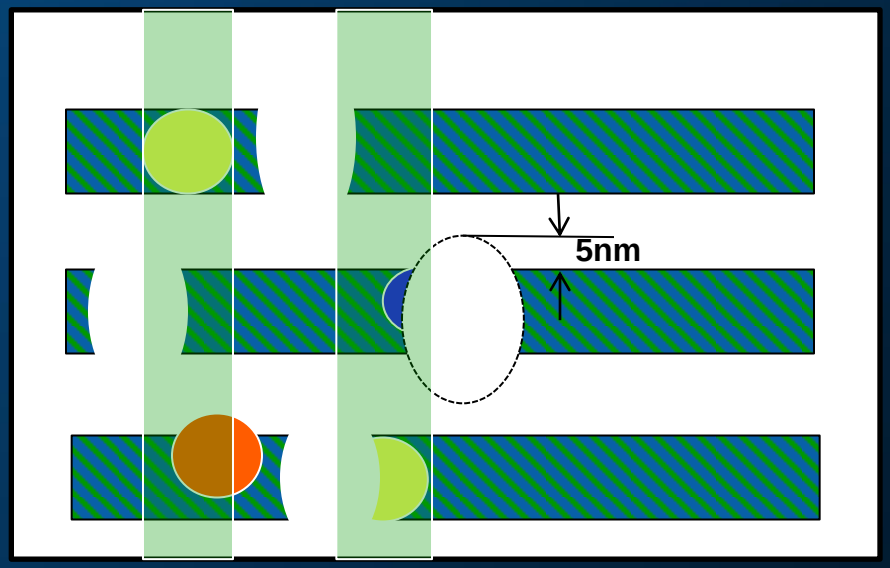
Assuming everything else = We would want at EUV or EB Insertion
EPE EUV or EB (OL, Stochastics) < EPE 193i (OL, Stochastics)

Complementary Lithography at Insertion Stochastics Suppression

EUV or EB Cuts and Vias



193i Cuts and Vias



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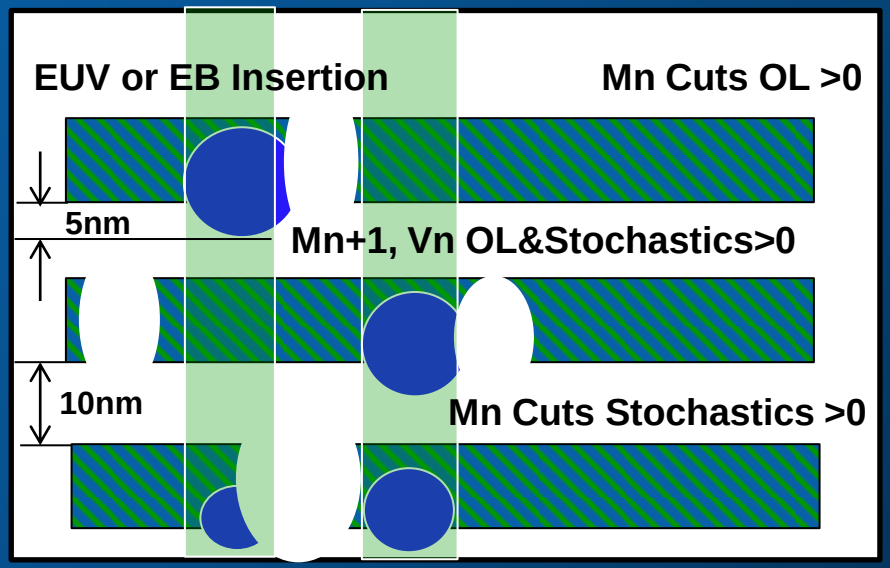
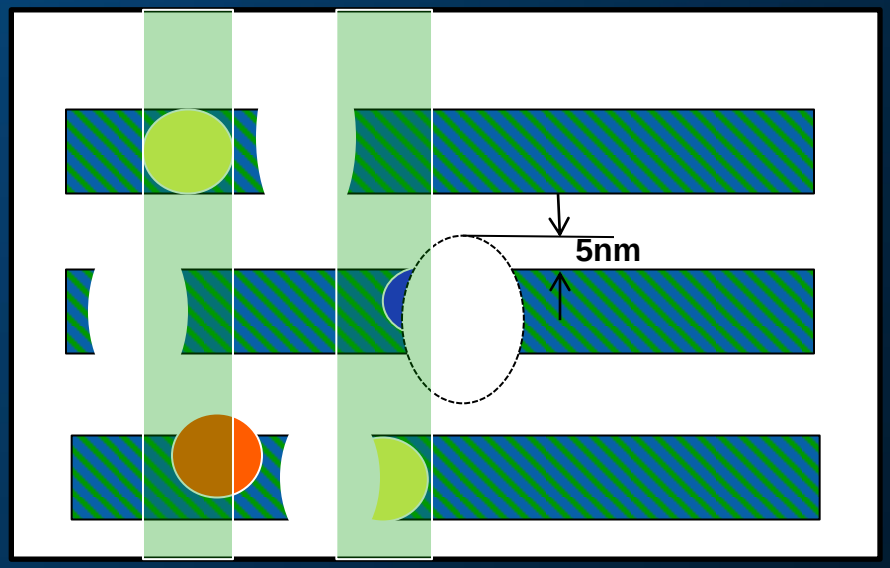
Complementary Lithography at Insertion Stochastics Suppression

EUV or EB Cuts and Vias



193i Cuts and Vias



EPE (EUV or EB/193i OL) ≤ EPE (N*193i/193iOL)

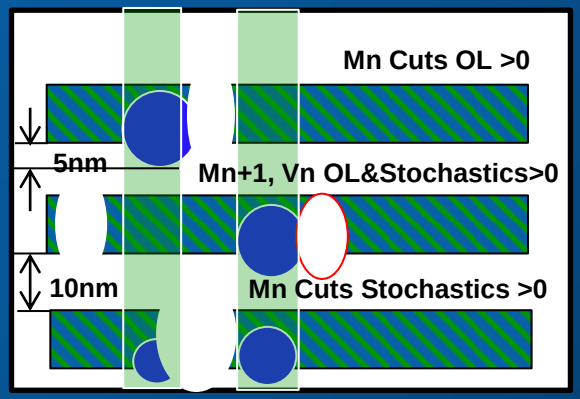
EPE EUV or EB Stochastics ≥ EPE 193i Stochastic

Assuming everything else = We would want at EUV or EB Insertion

EPE EUV or EB (OL, Stochastics) < EPE 193i (OL, Stochastics)

Given 5nm EPE_{All} limit what does it mean for EUV and EBDW Stochastics?

Complementary Lithography at Insertion Stochastics Suppression



$$EPE_{all} = EPE_{OL} \pm \tfrac{1}{2}\, CD3\sigma$$

$$|EPE_{all}| = EPE_{OL} + \tfrac{1}{2}\, CD3\sigma$$

CD3σ = f(resist stochastics, focus and dose errors, OPC Model and Correction errors, mask errors with MEEFs, Etch Biases, etc, etc, etc)

Assuming for simplicity for EUV and EBDW :

σ(resist stochastics) = σ(focus and dose errors, OPC Model and Correction errors, mask errors with MEEFs, Etch Biases, etc, etc, etc)

$|EPE_{all}| = EPE_{OL} + \tfrac{1}{2}\, CD3\sigma = EPE_{OL} + \tfrac{1}{2} CD3\sigma$(2resist stochastics)

or, keeping it simple,

$|EPE_{all}| = EPE_{OL} + CD3\sigma$(resist stochastics) = 5nm

Assuming EUV,EBDW/193i EPE_{OL}=2nm

$CD3\sigma_{EUV,EBDW}$(resist stochastics) = 5nm – EPE_{OL} =5nm-2nm =3nm

Complementary Lithography at Insertion Stochastics Suppression - EUV

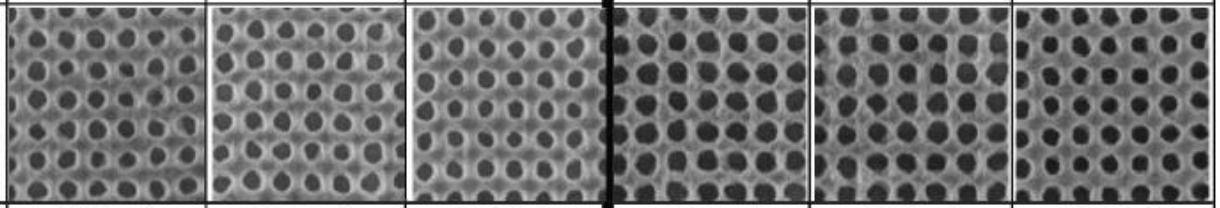
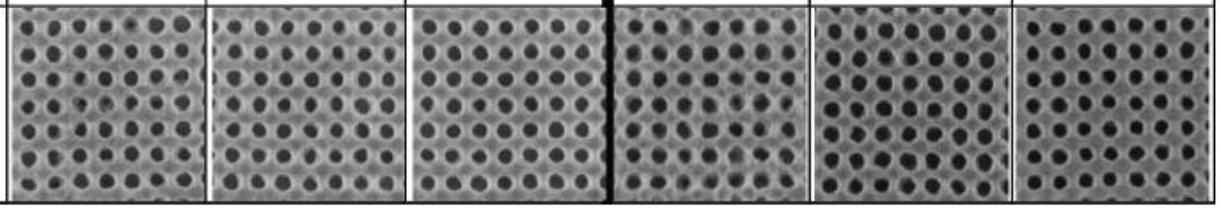
		Resist A	Resist B	Resist C	Resist D	Resist E	Resist F
Protecting group size		Bulky	Bulky	Bulky	Small	Small	Small
Protecting group ratio		Low	Middle	High	Low	Middle	High
35nm CH	Sensitivity	46.0mJ	55.9mJ	61.4mJ	53.2mJ	54.6mJ	56.1mJ
	CDU	9.7nm	5.8nm	3.6nm	Overdose	Overdose	3.8nm
	Top-down						
30nm CH	Sensitivity	50.1mJ	60.1mJ	70.6mJ	53.2mJ	59.5mJ	61.0mJ
	CDU	4.4nm	3.8nm	3.3nm	5.5nm	3.7nm	3.6nm
	Top-down						

Table 2. CDU values and sensitivity for different protective group ratios at 30nm HP and 35nm HP contact hole patterns. All six samples were exposed on the AMET using annular illumination. Process conditions are the same.

Key Parameters of EUV Resists for Contact Hole Applications

Prcs. of SPIE Vol. 8322, 83221B

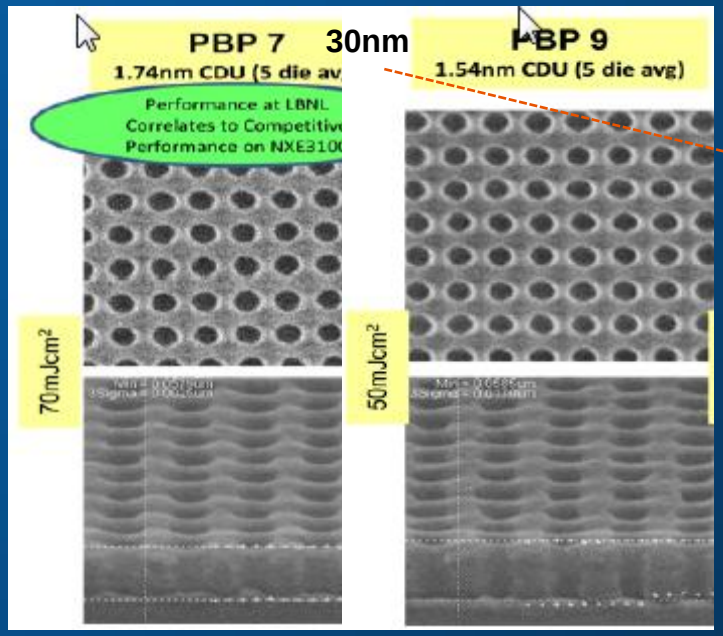
Kyoungyong Cho [1], Hiroki Nakagawa [2], Ken Maruyama [2], Makoto Shimizu [3], Tooru Kimura [3], Yoshi Hishiro [2],

[1] SEMATECH, 257 Fuller Road, Albany NY 12203
[2]JSR Micro, Inc., 1280 North Mathilda Avenue, Sunnyvale, CA 94809
[3] JSR Corporation, 100 Kawajiri-cho, Yokkaichi, Mie, 510-8552, Japan

$CD3\sigma_{EUV}$(resist stochastics) =3nm
For 20nm holes will be very tough!

Complementary Lithography at Insertion Stochastics Suppression - EUV

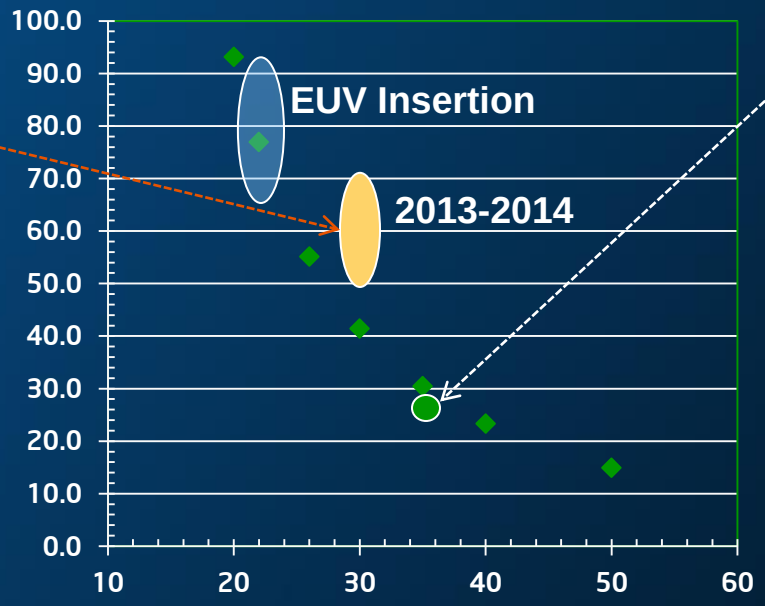
$CD3\sigma_{EUV}$(resist stochastics) =3nm = CD3σ (Photon, e^- Acid, Develop stats)



Comparison of EUV and e-Beam Lithographic Technologies for Sub 22nm Node Patterning

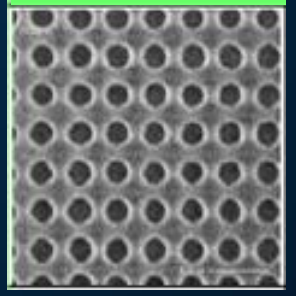
James Cameron et al 2012 Proc. of SPIE Vol. 8322 83222F-1

D_{inc} = Dose to Print (mj/cm²), Photon stats Only!



35nm, PBP 7

ASML NXE3100
Es 25.5mJ/cm²
BCDU [3 sig. (X/Y)]
3.2/3.03



`2

`1

$$D_{inc} \geq \frac{1.88}{\alpha \cdot \varepsilon} \cdot \left[\frac{2n}{EL \cdot S}\right]^2 mJ/cm^2$$

n=7
α=0.5
ε=2
EL=5%

Shot noise and process window study for printing small contact holes using EUV Lithography

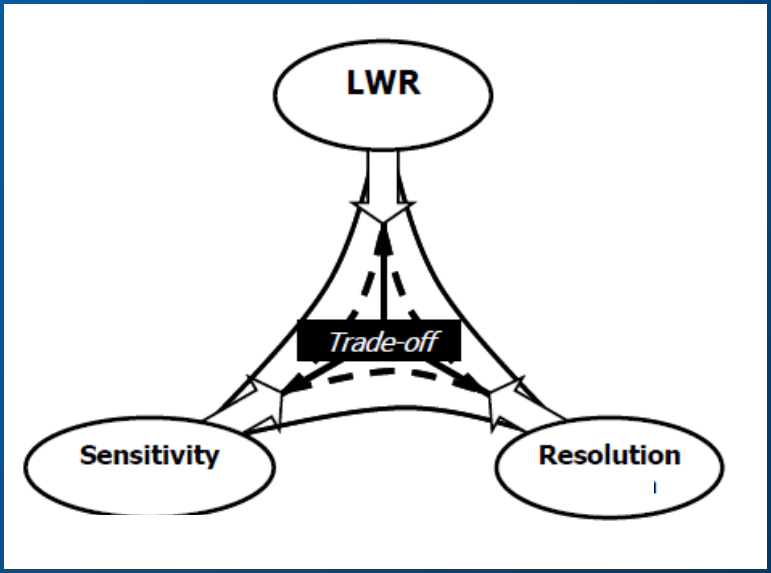
Sang H. Lee*, Robert Bristol, John Bjorkholm Proceedings of SPIE Vol. 5037 (2003)

`2

Yan Borodovsky, Intel, 2012

EUV Triangle

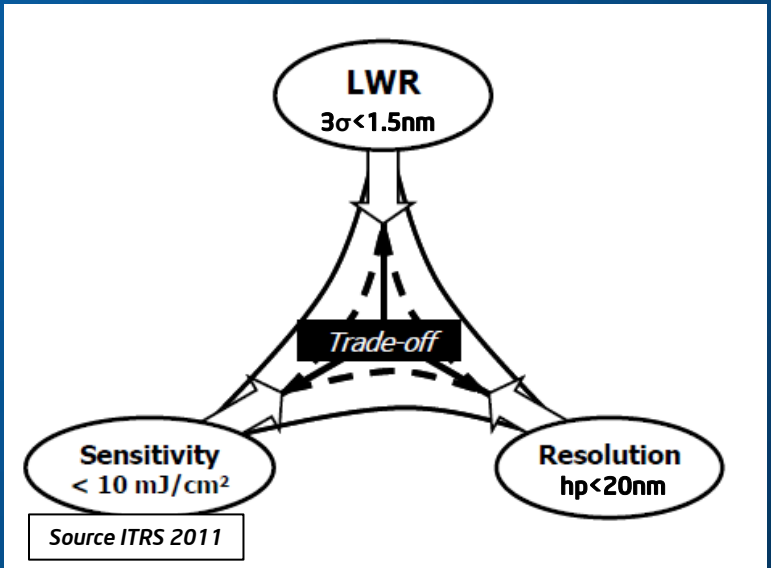
Line/Space



$Blur^3 * LER^2 * Dose = C$

EUV Triangle

Line/Space

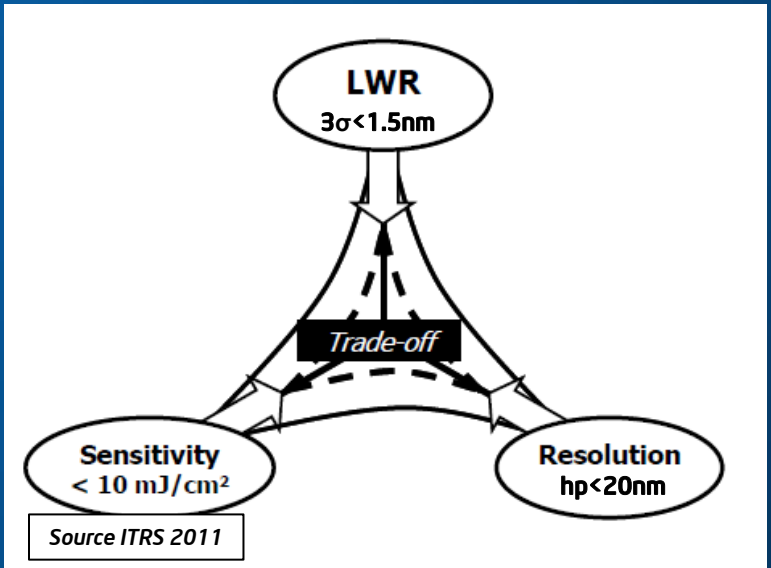


Blur³*LER²*Dose =C

Triangle of Death

EUV Triangles Duo

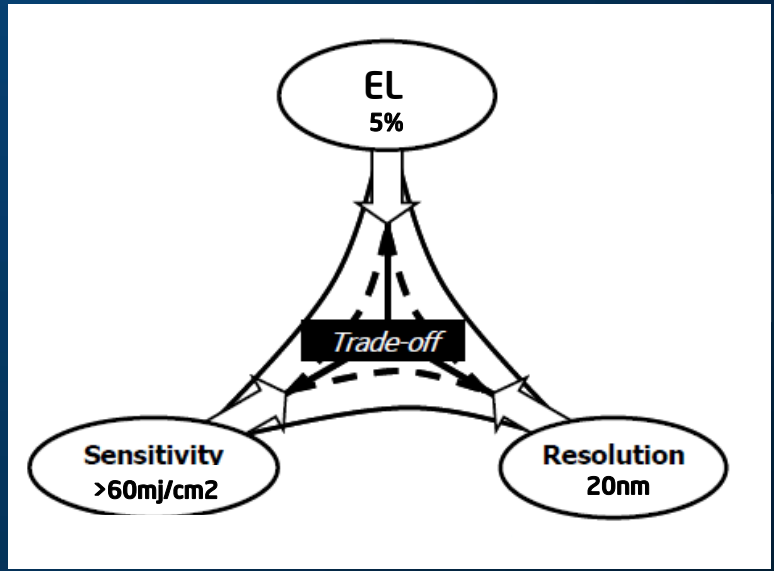
Line/Space



Blur^3*LER^2*Dose =C

Triangle of Death

Cut/Via

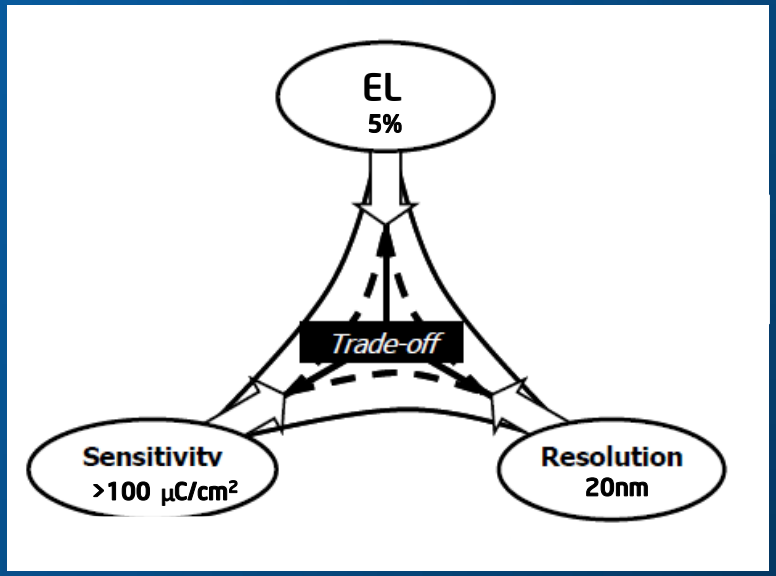


Size^2*EL^2*Dose=C

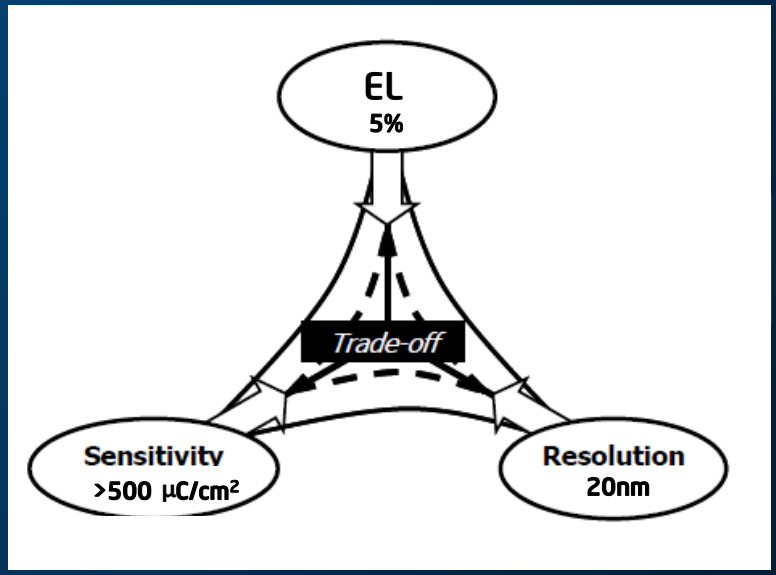
Triangle of Sorrow

EBDW Triangles Duo

Cut/Via for 5kV



Cut/Via for 100kV



$Size^2*EL^2*Dose=C$

Triangle of Sorrow

Complementary Lithography at Insertion Stochastics Suppression

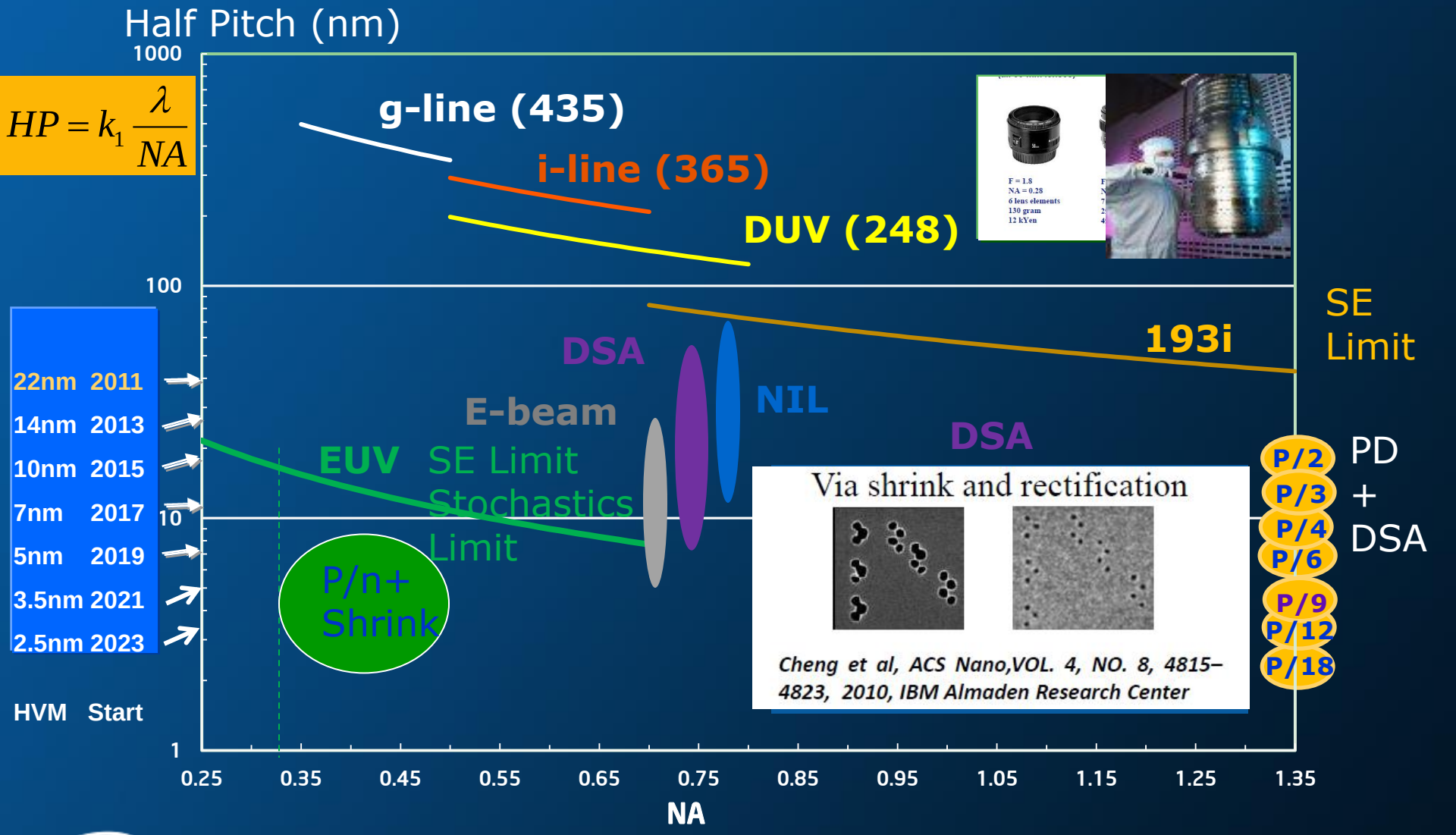
Photon Shot noise statistics alone leads to conclusion that resist capable to meet ~20nm Contacts and Cuts patterning at HVM might need to be sufficiently slower then current targets for EUV and EBDW.

It appears more and more IC manufacturers consider first EUV and EBDW HVM use as Via and /or Cuts patterning while resist requirements and scanner throughput are spec'd for line/space. Vendors and Customers need to agree on resist specifications for Cuts/Via patterning and required tools TPT to support beneficial EUV/EBDW COO at HVM Insertion.

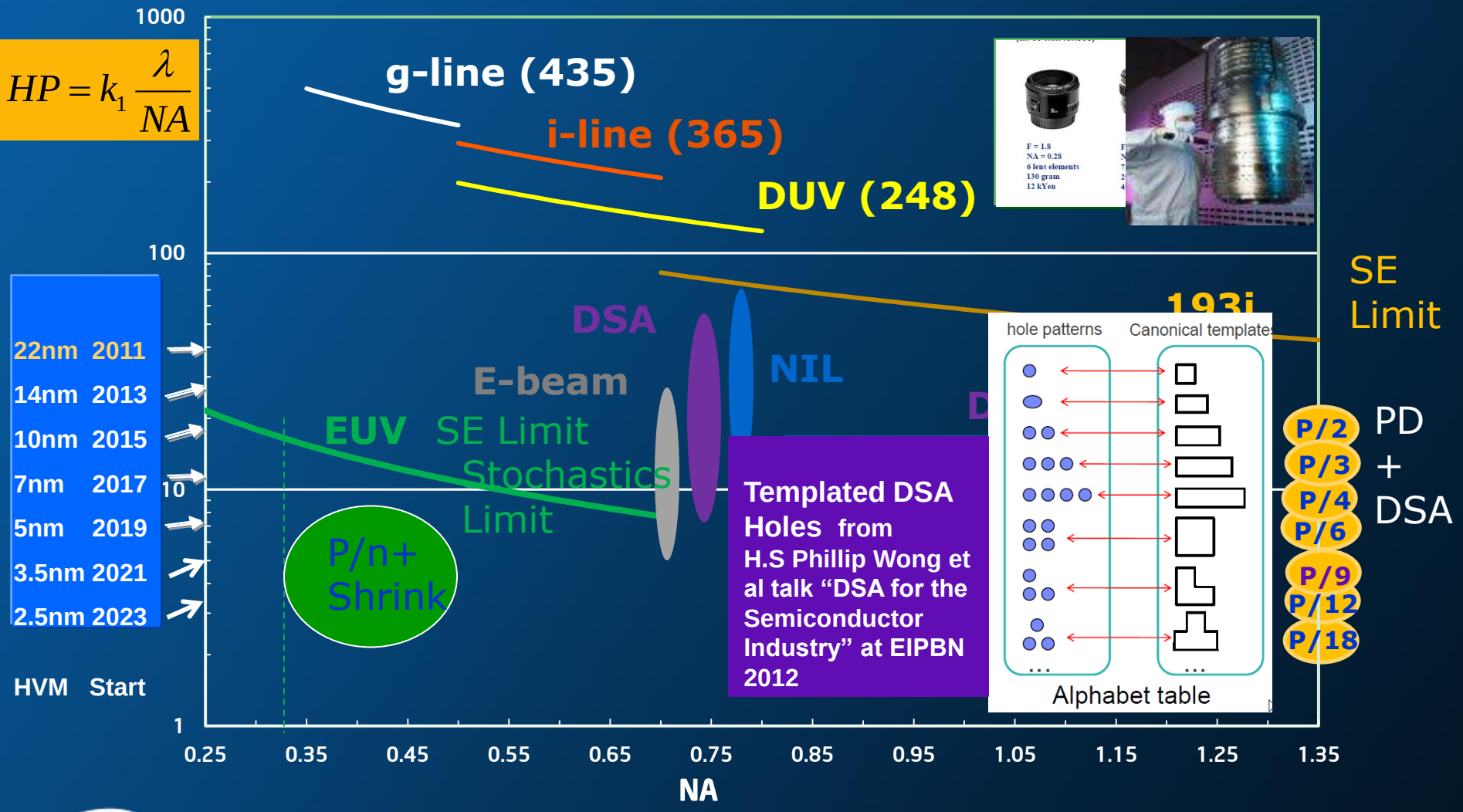
Need for Shot noise suppression that require progressively slower resists combined with technical challenges limiting HVM scanners throughput will most probably limit minimal dimensions of Vias and Cuts patterned in the resist by EUV or EBDW to ~20nm irrespectively of resolution advances that can be provided by respective tools optics.

Cuts and Vias <20nm will be achieved by shrinking techniques.

Lithography Limits- Cuts and Vias



Lithography Limits- Cuts and Vias



That's the Future - Complementary Lithography

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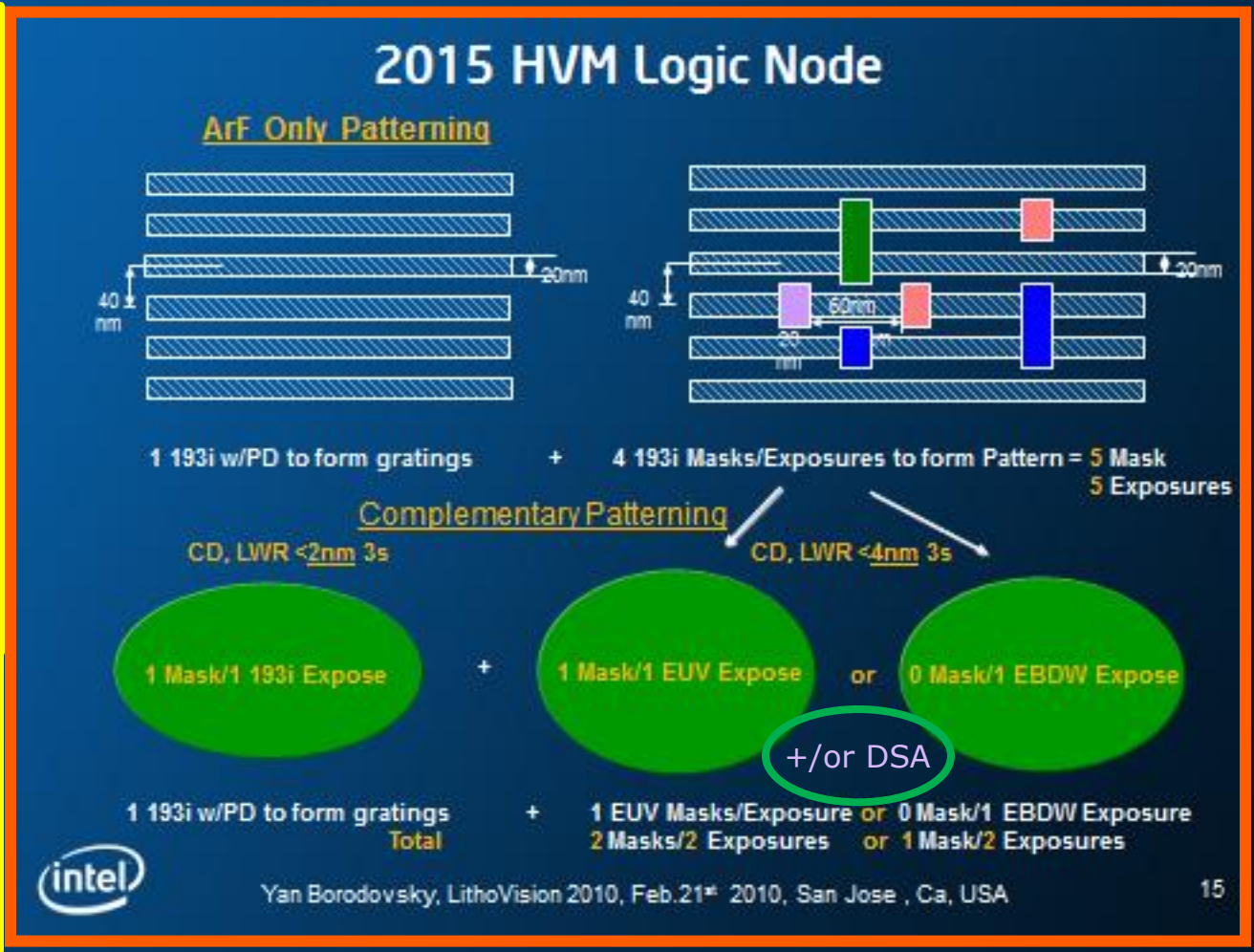
193i + Pitch Division
n*193i + Shrink Cuts
n*193i + Shrink Vias
before HVM NGL

Gridded Layouts –
193i + Pitch Division
n*193i or EUV Cuts
n*193i or EUV Vias
+Cuts &Via Shrink
with HVM EUV/EBDW

Gridded Layouts –
193i + Pitch Division
+ Cuts and Vias with
193i Templated DSA
with HVM DSA



Summary

Lithography Scaling will continue uninterrupted for foreseeable future. No fundamental technical or cost barriers foreseen.

193nm Immersion scaling will be extended for many Generations with Cost effective Pitch Division.

Regular Designs and Layouts will become ubiquitous.

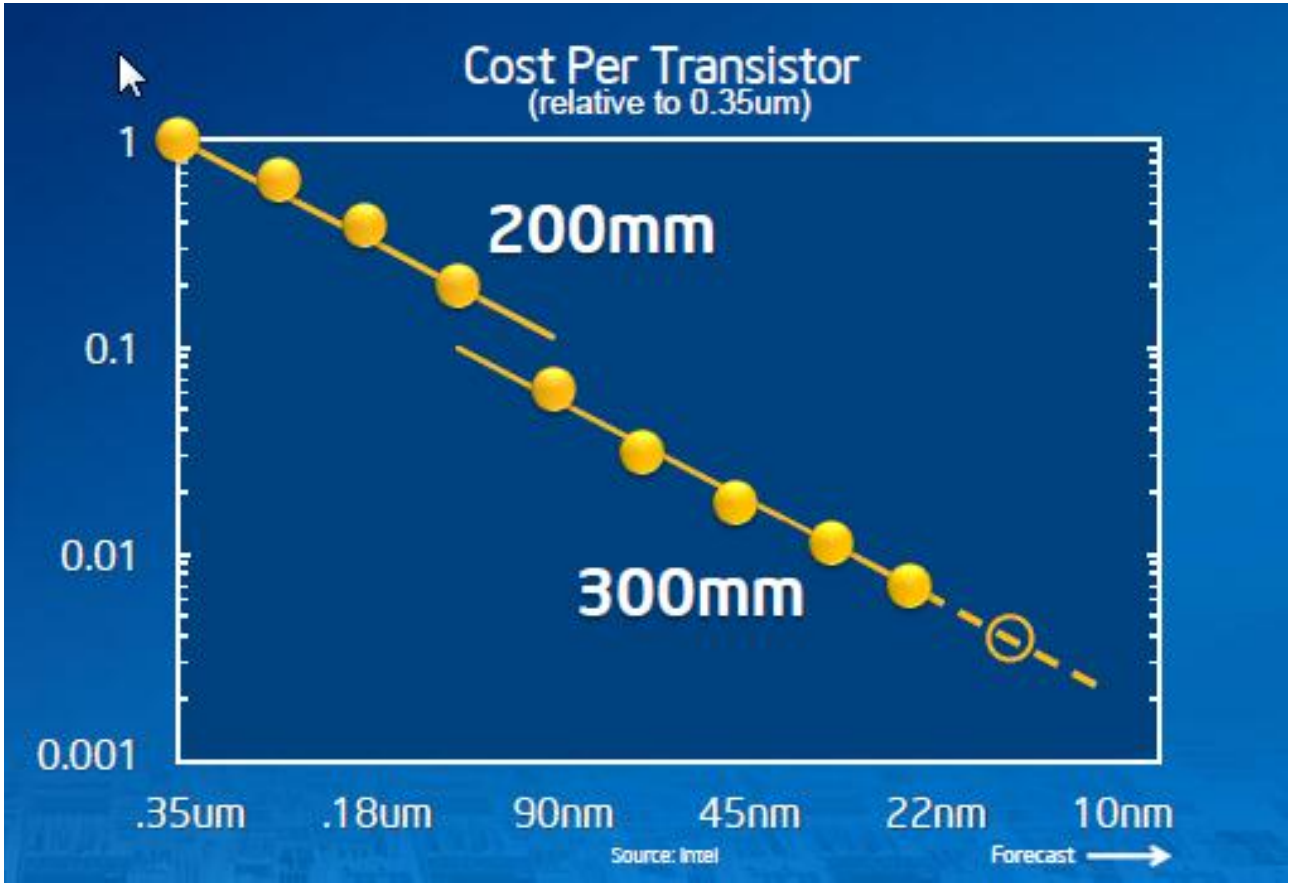
Complementary Technologies (DSA, EUV, EBDW) will be used to break gratings continuity and pattern Vias.

EUV and EBDW minimal Contact/Cut size will be ~20nm due to need for progressively slower resists to combat shot noise induced variability and Source Power, Columns current limitations.

DSA will be used extensively either in conjunction with 193i (Shrink, Templated DSA) or to shrink Cuts and Vias down while rectifying EUV/EB size variability induced by shot noise and other stochastics.

Backup

Past and Present



Cost Per Transistor on Historical Trend for 22nm, projected to be there for 14nm and 10nm nodes

EBDW Patterning

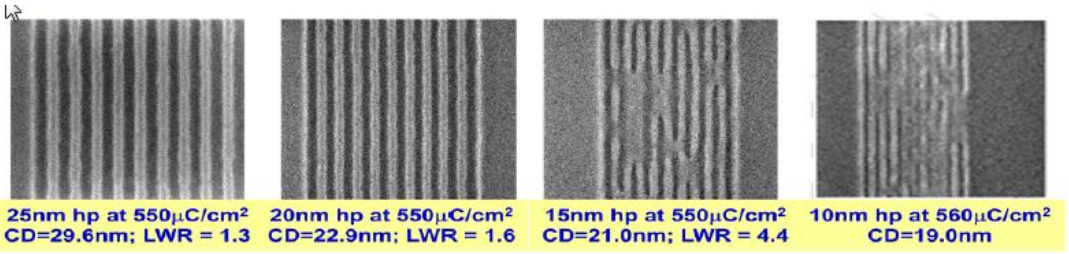


Fig. 6. Line Space and Contact Hole Patterning Capability with PBP 2 Resist using 100keV e-Beam Lithography.

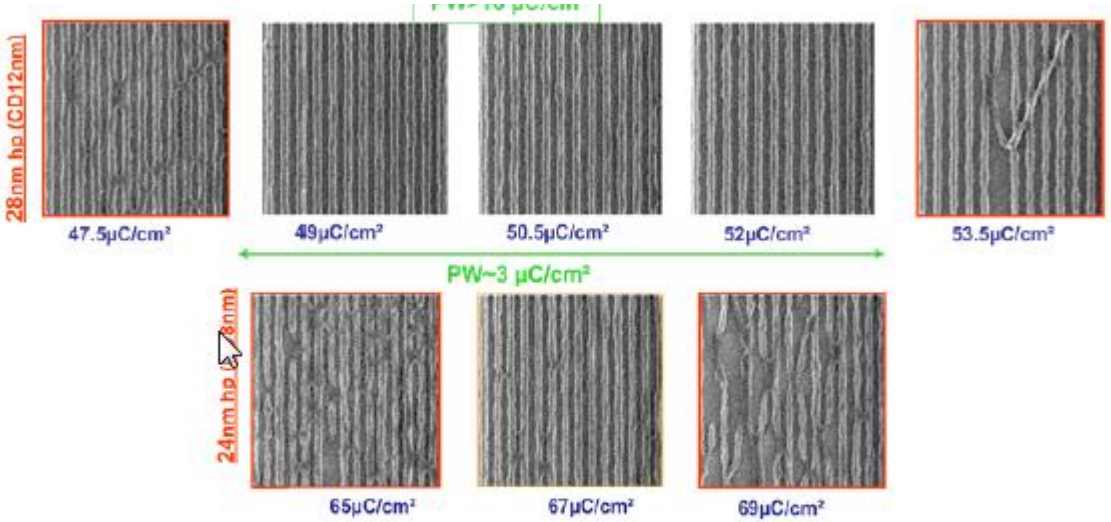


Fig. 7. Lithographic Performance of PBP 2 on MAPPER Pre-Alpha Tool at 5keV.

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EBDW Patterning

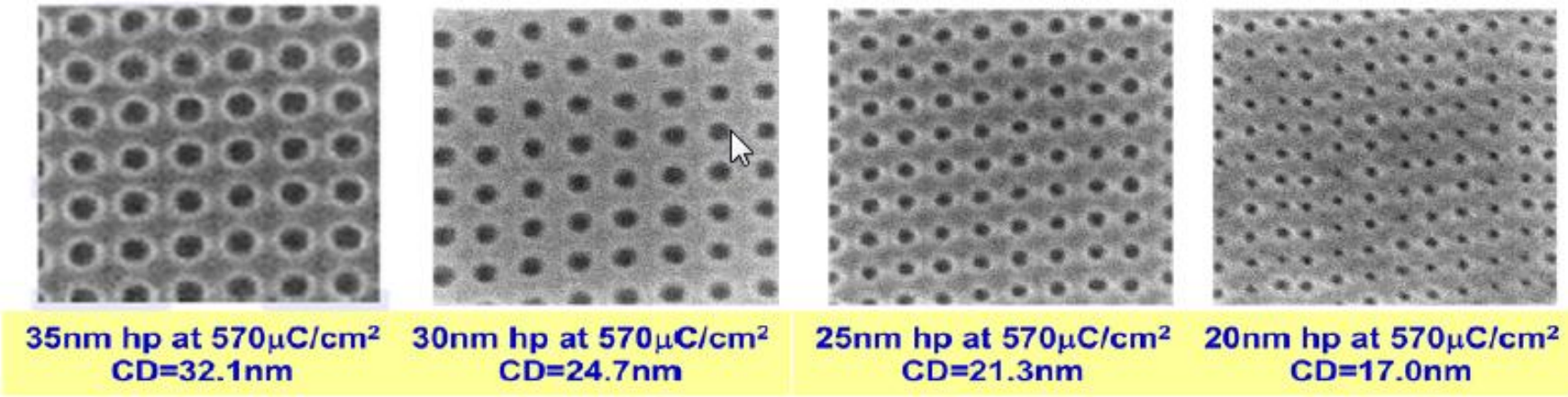

Fig. 6. Line Space and Contact Hole Patterning Capability with PBP 2 Resist using 100keV e-Beam Lithography.

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